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b) an encoder, arranged to encode the first parallel data to generate third parallel data of M bits (M≠ N);

c) a converter, arranged to convert the third parallel data into fourth parallel data of N bits; and

d) an error correction unit, arranged to selectively add an error correction check code to the second parallel data and the fourth parallel data,

said error correction unit performing a common addition processing irrespectively of second parallel data and the fourth parallel data. –

Cancel claim 34.

Amend claim 37.

-- 37. (Amended) A digital information coding method, comprising:

selectively inputting a first parallel data of N bits representing a first digital information and second parallel data N bits representing a second digital information, wherein a bit rate of the first digital information differs from a bit rate of the second digital information;

encoding the first parallel data to generate third parallel data of M bits (M ≠ N);

converting the third parallel data into fourth parallel data of N bits; and

selectively adding a predetermined data amount of error correction check code for every predetermined data amount of to the second parallel data or the fourth parallel data,

said adding step performing a common addition processing irrespectively of the second parallel data and the fourth parallel data. –.



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